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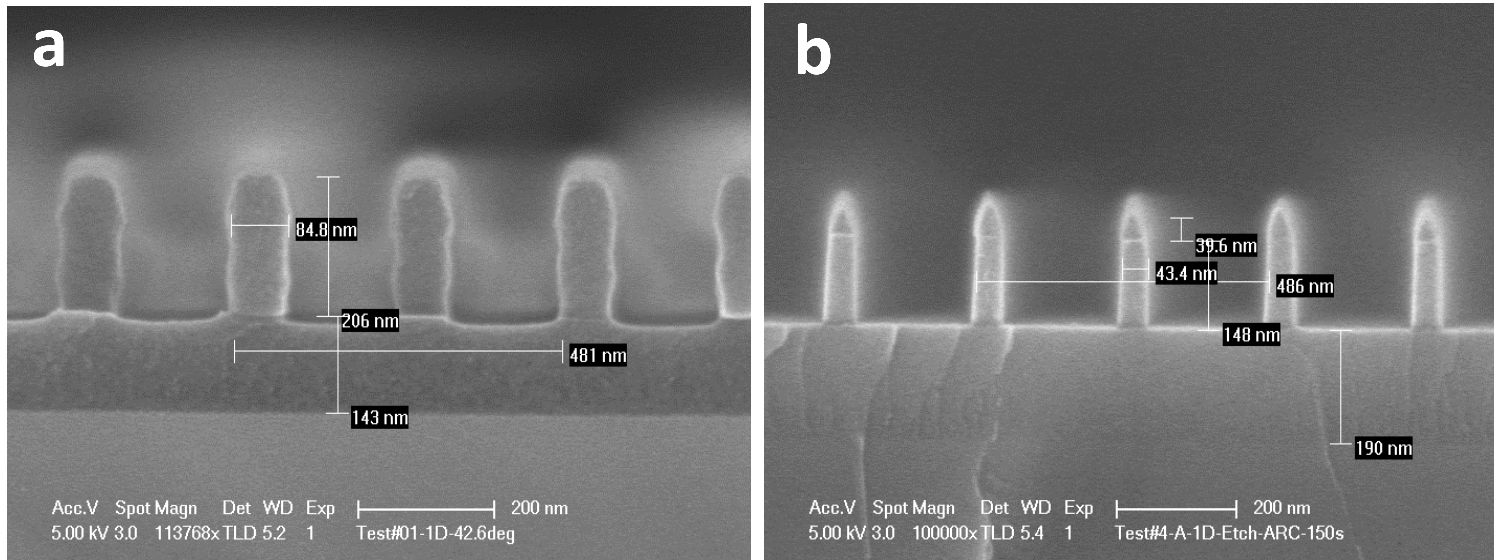
SiO_2 Nano-Structure Etch

1)1D-Trench-Line pattern created using Holography
Sample: PECVD- SiO_2 (~190nm) on Si

Figure 1. (a) 1D-trench-line resist pattern after holography (θ=42.5°); (b) 1D-trench-line pattern after transferring from PR to ARC using RIE#5 with 5mT, 150W, O_2=20sccm, and time=150s.



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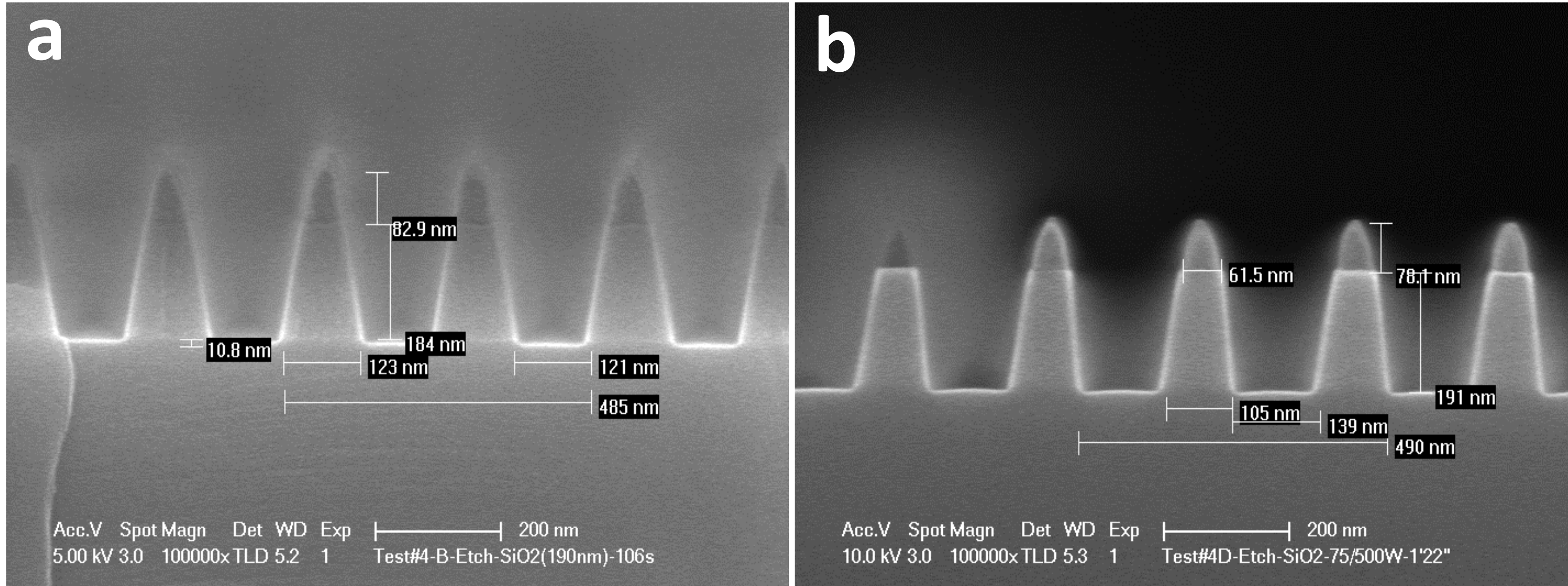
2) SiO_2 Etch using Panasonic ICP#2

Table 1. SiO_2 Etch Result

SiO_2 Etch using Panasonic ICP#2 Tool										
Recipe#	Pressure (mT)	Power (W)		Gas Flow-rate (SCCM)			Etch Rate (nm/min)	Side-wall Angle (°)	Micro-trench
		Bias	ICP	CF_4	CHF_3	O_2			
1	0.5	50	900	20	20	0	107	76.3	no (see Fig 1(a))
2	0.5	75	500	20	20	0	131	83.5	no (see Fig 1(b))
3	0.5	200	900	0	40	0	290	84.2	no (see Fig 1(c))
4	0.5	100	900	20	20	0	198	80	no (see Fig 1(d))
5	0.5	50	900	20	20	10	101	74.3	yes (see Fig 1(e))
6	0.5	50	900	30	10	0	106	85.5	no (see Fig 1(f))
7	0.5	50	900	40	0	0	110	83.4	yes (see Fig 1(g))

Figure 2. SiO_2 Etch Profiles: (a) 0.5Pa, 50/900W, CF_4/CHF_3=20/20sccm, 106s; (b) 0.5Pa, 75/500W, CF_4/CHF_3=20/20sccm, 82s; (c) 0.5Pa, 200/900W, CHF_3=40sccm, 39s; (d) 0.5Pa, 100/900W, CF_4/CHF_3=20/20sccm, 57s; (e) 0.5Pa, 50/900W, $CF_4/CHF_3/O_2$=20/20/10sccm, 113s; (f) 0.5Pa, 50/900W, CF_4/CHF_3=30/10sccm, 108s; (g) 0.5Pa, 50/900W, CF_4=40sccm, 104s.



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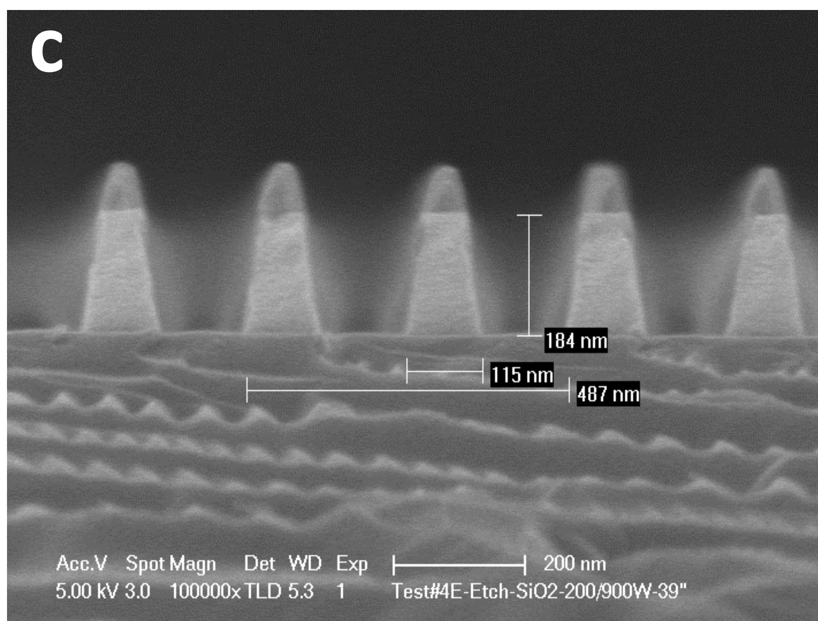

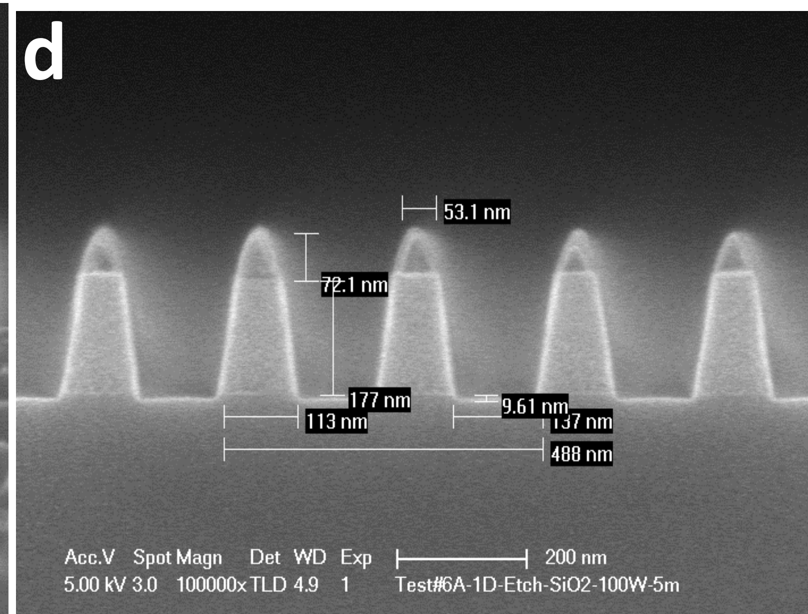

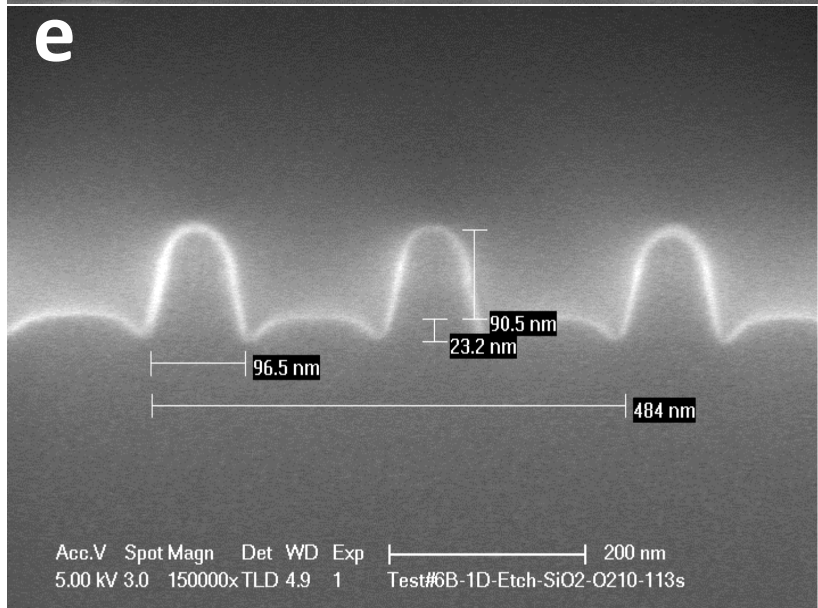

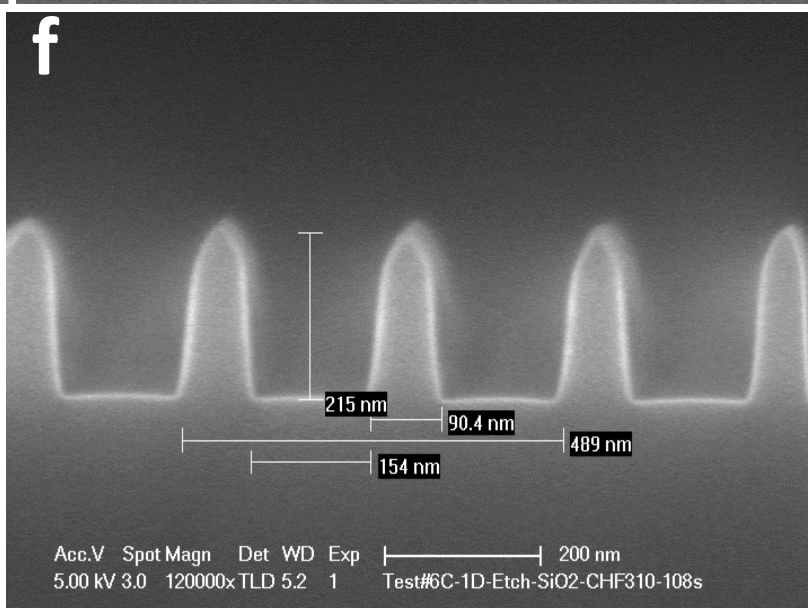

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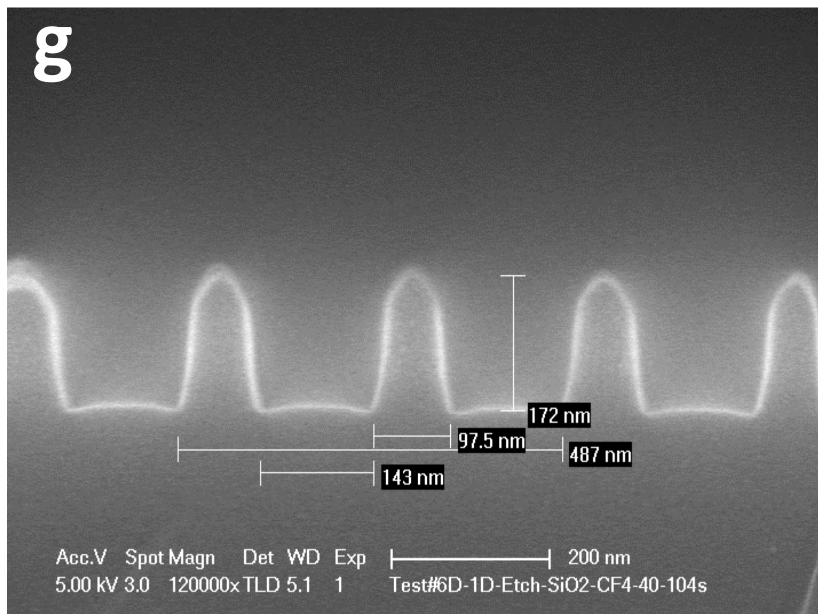
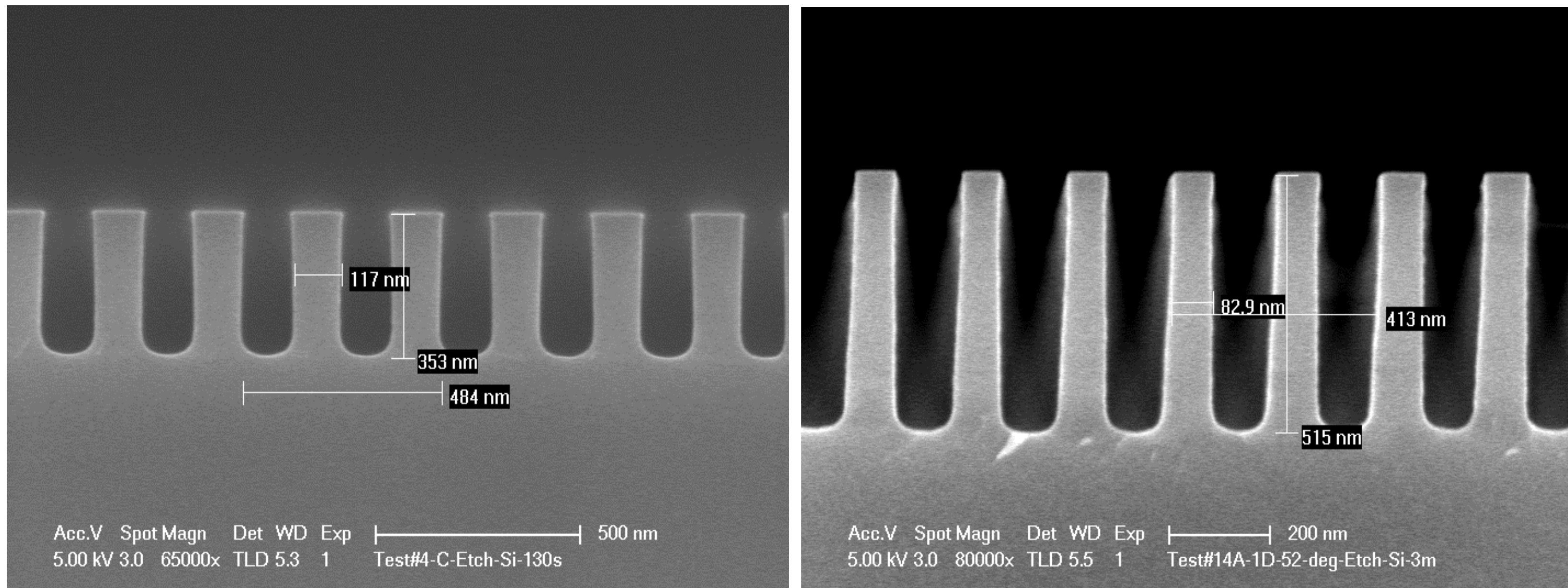


3) Etch underneath Si using SiO_2 as a Mask (now, one can use above SiO_2 Line, with a different side-wall angle, as an etch mask to etch Si line with a different line-width).

Figure 3. Si etch profile using DRIE with 19mT, 15/825W, $SF_6/C_4F_8/Ar$=26/54/20sccm: (a) using SiO_2 profile Fig 2(a) as a mask: Si line-width=117nm; (b) using SiO_2 profile Fig 2(f) as a mask: Si line-width=83nm.



Note: One can get a similar result of 2D nano-post with a different post diameter using a different SiO_2 etch-mask profile.